The Full Circuit Service

Elegant solutions to difficult problems

Full Circuit provides a full electronic design service of expertise and equipment. Its wealth of expertise will tell in the reliability of your end product as Full Circuit has a very high success rate in 'Right 1st Time' designs. Coupled with a fixed price means that not only are your overall costs reduced but they are also more controlled. Or if the contract is time and materials then Full Circuit's extensive experience means the job is completed in short time.

The core expertise covers the areas of:

- Analogue – including: transformers, LC filters, gyrators, etc.
- Power Electronics – including: switch mode and linear power supplies, High Voltage and Low
- Digital - including: embedded micros, VHDL IP and obsolete component substitutes
- Simulation – including: Pspice/Spice
- Railway Electronics - including: track circuits, ATO, ATP, Interlockings.
- Railway Simulation - including: track circuits on AC or DC traction.
- Software - including: embedded assembler, C, C++.
- Prototype PCB Layout.

In addition to this core Full Circuit has working arrangements with other companies for skills outside the core, RF, ASIC, should you require a complete package of work.

There is no minimum contract period so our working relationship could start with a short trial contract. Whatever way the contract is arranged I am confident that the quantity and quality of the work will meet your expectations. Please email or phone (on +44 1249 720161) so we can discuss your requirements.

Malcolm Reeves, BSc CEng MIET MIRSE

Director, for and on the behalf of, Full Circuit Limited

{ see: http://www.fullcircuit.com for more details}

Curriculum Vitae

Personal Details

Name: Malcolm Robin Reeves

Address: Chippenham, Wiltshire, England

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Phone +44 1249 720161

Age: 56

Status: Married, 4 (grown up) children

Qualifications

O Levels:	5	English, Physics, Mathematics, Chemistry & Biology
A Levels:	3	Physics, Applied Mathematics & Pure Mathematics
BSc (Hons)		Electronic Physics, University of London
City & Guilds	2	C Programming II and C++ Programming III (refreshers)
Memberships:		The Institution of Engineering and Technology, Chartered Engineer The Institute of Railway Signal Engineers

Strengths

Innovation. Analogue Design. Digital Design. Simulation. Fail-Safe & Safety Design. Switch-Mode PSUs. Filter, Transformer & Inductor Design. Embedded Processors. EM Immunity. Track Circuits & Railway simulation. Design for Industrial Environments (Temperature, Vibration, EMI etc.). VHDL, SPICE, Assembler, C.

Other Information

Computer Languages:	C++, C, Pascal, Delphi, Basic, HTML, CSS, PHP, Javascript, JSD, Assembler for 186, 8086, 6800, 6502, 9995, PIC, ARM
Computer Applications:	Word, Pspice, MathCAD, Power Point, Excel, Timing Designer, OrCAD, Mentor Expedition.
Procedures:	Familiar with ISO9001, QMS, EDM, ENVs on EMI, FMECA, FTA.
General:	5 patents (sole named inventor). All my designs that I have taken through to production have been successful and those at Westinghouse and later have had fully detailed analysis documents to support them. I have had a Railtrack PTS. I am familiar with DSP, the latest SM PSU techniques, embedded modems and DAA, low power radio and ARM.
Examples:	Detailed discussion of key projects and patent details can be found at http://www.fullcircuit.com/projects.htm . Also on this site are free examples of my software skills.

Experience (in reverse order)

Employer: Full Circuit Ltd

Business: Consultancy Design (my company)

Period: August 1996 to date

Project	**Technically Responsible for :-**
M9	2013. A complete rewrite, in 3 weeks, of ARM SBC software with Ethernet IP stack together with real time ADC sampling. Software included debug routines which later proved their worth again in prototype setup.
ROM12	2013. Feasibility study on minimum changes/practicality of ROM working voltage change (50V to 12V). Transformer redesign and component selection. System simulation leading to VHDL changes to suit new design. Prototype testing.
SOM110	2012/2013. Design, hardware analysis and EOLA (Enviromental Operating Limits Analysis) reviewing.
ROM	2010/11. Rail signalling relay output module. Floating outputs, switch mode based, SIL4 design. Responsible for concept, circuitry, transformer design, VHDL safety concepts, parts of the VHDL coding/design
CIM	2010. Rail coded input contact proving module. Transformer design (400/800Hz). Manchester encoded signal for contact proving. SIL4 (safety) design. Improved and maximised wetting and reliability. Well defined, testable and proved closed/open loop impedances
POM	2009/10. Rail points machine direct drive module. AC input, forward and reverse outputs, 120Vdc, 28A. Safety concepts, circuitry design including heatsinking. VHDL safety concepts and design.
JTC Osc	2009. Jointless Track Circuit Unit oscillator problem study and retro-fitted fix design.
WESLED	2009. LED signal lamp replacement. Revised yellow variant analysis.
CIM/SOM	2008. Rail signalling input and signal module outline concepts and design.
SSI TFM	2007. Rail SSI TFM EMI issues study and analysis. Finding the root of EMI induced problem and designing a solution.
JLTC Set-up	2006. Rail Joint-Less Track Circuit set-up and maintenance tool. Rail inductance measurement plus other diagnostics. Hand-held, battery powered, graphic display and keypad. Self-testing and calibrating. PIC DSP processor based. Gyrator based narrow band filters. Responsible for whole design, concept, circuitry, mechanic packaging, software, VHDL for cpld's and PCB layout. Plus build of 10 units.
WESLOCK	2005. Rail safety sensor of isolated current and voltage. Design, analysis, modelling and prototyping.
WESLED	2005. LED signal lamp replacement. Blue variant analysis.
X10-RS232	2005. Low cost PIC based X10 mains signalling to/from RS232, including mechanical design concept. Novel I/O filter design, low cost, high performance. Output designed for EN50065.
Pwr Ctrl	2004. PIC based interface. Inputs: switches and signals. Outputs: relay drives and signals. Software State Machine with switch debounce, timing functions and watchdog for robust operation. Power usage minimised.
PPAM	2004. High frequency Class B power amplifier (0dB 1MHz). Tuned loop load via up to 2.5km of cable. Stable under all conditions. Design achieved distortion well below 0.01% specification.
LMM	2003. FSK Loop modem. Designed with filters using Gyrator and NFDR versions of LC ladders for stability, defined characteristics, and long available life expectancy. CPLD used for FSK generation and decoding. CPLD also for VME interface.
ACOL PSU	2003. 115V 400Hz and 28Vdc PSU for LED Anti-Collision light. Energy storage to spread flash surge. Constant current output regulation. Extremely accurate flash time to ensure synchronisation between separate units.

UAIS	2002. Main and display PSUs running off ship's battery and to meet EMC requirements.
WESLED	2001. LED signal lamp replacement. 110V input, sinewave current load. DC current output, temperature compensated to give constant light level. LED PCB thermal design and analysis.
LED Reg	2001. LED lamp close tolerance constant current regulator. The impossible of 4 regulators, one matching a temperature compensation curve, over 70W dissipation, all in a 20x30x12mm volume (in surface mount not hybrid).
9902IP	2000. VHDL IP, design and test, for replacement of obsolete uart/timer ic with cplds. Including difficult mechanical and layout design to fit in 18 pin DIL footprint.
VLC5	2000. FMECA of VLC5 vital processor based module.
9995/02	2000. Investigation into CPLD, FPGA, ASIC, etc. replacements for TMS9995 processor and TMS9902 UART with costings.
VLM	2000. Analysis of VLM software performance, identifying bottlenecks. Streamlined code to give factor of 2 processing improvement. Analysis of hardware to define best option for future speed improvements.
VROM	1999. Analysis of algorithm/hardware problem which was causing infrequent but costly failures. Re-designed algorithm to be stable and more noise immune. Analysed noise disturbance worst case to prove recovery in time allowed.
Spice	1999. Creation of two C++ classes (MS Visual C++) to add Monte Carlo and Worst Case analysis to spice simulation program.
Oslo	1999. Analysis of Oslo railway environment and GPOM to track down failures only occurring once every two months (extensive site tests and lab measurements).
Gap Gun	1999. Re-design of parts of a laser and camera 3D scanner to correct problems (surface mount plus tight space constraints). Design of new 3 channel video digitiser for SBC or PC, variable resolution in width and height. Schematic and detailed layout guidelines (IC placement, pin allocation, general routing areas, 0V connections and plane splits).
TBS	1998. Design analysis and simulation of inductive loop system (power amp, PLL decoding FSK). Creation of (spice ac) model of switched capacitor filters.
FS2000	1998. Design analysis identifying the cause of failures and the design of solutions. Various areas of train equipment (ATO and ATP) covering life prediction, PLL, comms, filters, relays, opto-isolators, and general digital.
TX9000	1997/8. Design of calibration equipment with low drift (0.1%) yet to take high power pulses (3kW). Other parts with even lower drift (125ppm but less power). Design of dual slope ADC and precision temperature measurement.
FS2600 Track Circuit	1997. Simulation of track circuit to develop fixed set-up method for Australia.
FS2700 Track Circuit	1996/7. Design of filter element between transmitter (signal generator) and track to make workable track circuit. Simulation of FS2700 performance (including EMI) on railway. Technical support for other FS2700 component design teams.

Employer: Westinghouse Signals, Chippenham, Wiltshire, UK

Business: Railway Signalling Equipment

Period: October 1982 to July 1996

Project	**Technically Responsible for :-**
FS2700 Track Circuit	1996. All system and outline design including new features of heterodyne via lookup table for narrow and site selectable filter (pre complex FFT). The most difficult analogue and digital design areas. Designs include; switch mode PSU,, output matching filter, safety proving circuit.
FS2550	1996. Outline design (which reused a lot of FS2600). Part of analogue design and

Track Circuit	the new safety proving circuit (digital). 1 patent taken out.
FS2600 Track Circuit	1993 - 1995. All system and outline design. The most difficult analogue areas including input filter, total 21st order, with heterodyne stage (pre FFT). Most of the system simulation and the new features. Presented these innovations in a joint paper with a colleague at Aspect 95 and 2 other venues.
General Purpose O/P Module	1993. Outline design to solve extremely arduous requirements. All detailed design including embedded processor, A/D, output stages, using mosfets for PWM dimming, with hall effect current sensors.
FS3000 Track Circuit	1992. Generation of new track circuit ideas. 2 patents taken out. On going, staged development.
Westrace Interlocking	1988 - 1992. All parallel output, ac-dc mosfets, and input design (fail-safe). 2 patents taken out (3 for the entire system). Master fail-safe output design. Fixed loop time software routine design.
SSI	1987. Self test software using loop back and software UART. Site tests in Hong Kong.
FS2000 ATP	1982 - 1986. Embedded processor design, added innovation of fault reporting using NV ram and mini printer. Software and hardware of site test box, performing FFT, with LCD display of results. Technical support for (successful) sales team in Singapore

Employer:	Unitek, Abercarn, Gwent, UK
Business:	High Vacuum Deposition Equipment
Period:	December 1980 to October 1982
Project	**Technically Responsible for :-**
Vacuum Despositer and Plasma Sputterer	Various power supplies, 4kW, 5V to 13kV; fibre optic data links; PID control loops, D/A, A/D, all with high EM immunity. These used diverse components, SCRs, transductors, water cooled valves as well as the usual CMOS logic and op-amps.

Employer:	Techicon Isca, Crosskeys, Gwent, UK
Business:	Bulk Weighing Equipment
Period:	October 1978 to January 1980
Project	**Technically Responsible for :-**
Bulk weigher and flow controller	Re-design of microprocessor based weighing equipment to pass Board of Trade requirements and to improve reliability. New display unit. Battery inverter for ac motor. Technical support for sales team in Algeria.

{ For the latest version and examples of my work, see: http://www.fullcircuit.com }